REMARKS

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, has tentatively rejected all claims 1-13. In response, to the Office Action, Applicant has amended the specification to make a certain minor typographical and editorial revision. This Amendment also revises claims 1, 5, 7, and 10-12. Specifically, independent claims 1, 5, 7, and 10 have been amended to clearly define over the cited art of record. Applicant respectfully requests reconsideration for at least the reasons set forth herein.

The Office Action rejected claims 1-13 under 35 U.S.C. § 103(a) as allegedly unpatentable over Applicant Admitted Prior Art (AAPA) in view of LaBerge (U.S. Patent No. 6,615,345). Among claims 1-13, claims 1, 5, 7, and 10 are the independent claims. Claim 7 is directed to an apparatus and claims 1, 5, and 10 are directed to method embodiments. In view of the amendments made herein, Applicant respectfully requests reconsideration and withdrawal of the rejections.

The rejection advanced against the independent claims 1, 5, 7, and 10 was set forth in a single paragraph, effectively treating the application of the cited reference equally against each fo these claims. Therefore, Applicant will respond in kind. As amended, herein, independent claims 1, 5, 7, and 10 respectively recite:

1. A method for determining a common write delay time of a memory in a computer system, comprising a north bridge chipset and a BIOS (Basic Input/Output System), said method comprising the steps of:

enabling said north bridge chipset to determine a write delay time;

issuing a write command directly from said north bridge chipset to said memory for writing a pattern to said memory;

directly writing said pattern to said memory by said north bridge chipset according to said write command after said write delay time elapsed;

enabling said BIOS to read said pattern stored in said memory; and

enabling said BIOS to check whether said read pattern in said memory meets said corresponding written pattern, wherein said write delay time is passed if yes, and finally determining said common write delay time according to at least said write delay time which is passed.

5. A method for determining a common write delay time of plural ranks of memories in a computer system, said computer system comprising a north bridge chipset and a BIOS (Basic Input/Output System), said method comprising the steps of:

(a) selecting one of said ranks of memories;

(b) writing a pattern into said selected rank of memory according to different plurality of write delay times, comprising :

selecting one of said write delay times;

issuing a write command to said rank of memory for writing said pattern into one block of said memory; and

directly writing said pattern into said corresponding block by said north bridge chipset according to said write command after said selected write delay time has elapsed;

(c) repeating steps (a) and (b) to write said pattern into said ranks of memories according to said write delay times; and

(d) enabling said BIOS to read said pattern stored in said ranks of memories, determining a write delay time range of each rank of memories according to correctness of said read pattern, and then determine said common write delay time.

7. An apparatus for determining a common write delay time of a memory, comprising:

a CPU;

a north bridge chipset electrically connected to said CPU and said memory, ***said north bridge chipset for directly controlling writing of a pattern into said memory according to a plurality of different write delay times***;

a south bridge chipset electrically connected to said north bridge chipset; and

a non-volatile memory for storing a BIOS (Basic Input/Output System), wherein the BIOS is executed for reading said pattern stored in said memory and checking correctness of said read pattern to find a write delay time range of said memory and to determine said common write delay time.

10. A method for determining a common write delay time of a memory in a computer system, said computer system comprising a north bridge chipset and a BIOS (Basic Input/Output System), said method comprising the steps of:

directly issuing, from *said north bridge chipset,* ~~***to issue***~~ ***a write command to said memory so as to write a pattern to said memory according to a write delay time***; and

enabling said BIOS to check whether said pattern stored in said memory meets said written pattern, wherein said write delay time is passed if yes, and said common write delay time is determined according to at least said write delay time which is passed.

(*Emphasis added.*) Claims 1, 5, 7, and 10 patently define over the cited art for at least the reason that the cited references, even when combined, fail to disclose at least the features emphasized above.

In rejecting these claims, the Office Action relied principally on the AAPA and secondarily on teachings of LaBerge. The Office Action acknowledges that the AAPA, "[page 2, paragraph 0003 – page 4, paragraph 0008]" (as indicated by the Office Action) fails to disclose all the features relating to the north bridge chipset, as the rejected claims variously require. However, the Office Action points to LaBerge as allegedly disclosing "a computer system utilizing the north bridge in adjusting the write delay time in memories [Fig. 7; col. 3, lines 6-16; col. 4, lines 36-65]." The Office Action asserted that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to determine and adjust the write delay time in memories." The Office Action additionally asserted that "it is more advantageous to utilize the north bridge in determining and adjusting the write delay time of a memory because the north bridge is physically more closer to the processor and the system memories [Fig. 7]." Applicant respectfully disagrees.

In determining obviousness, it is impermissible to pick and choose from any one reference only so much as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such references fairly suggest to one of ordinary skill in the art.

Applicant respectfully disagrees with the rejection and submits that the combination of the AAPA and LaBerge, proposed by the Office Action, does not properly teach or even suggest all features required by the claimed subject matter, as in amended claims. In addition, nothing in the either of the applied references suggests the proposed combination by the Office Action to arrive the claims rejected.

In the rejection, the Office Action acknowledges that the checking method taught by AAPA is performed by a CPU executing the BIOS, which fails to teach all features of the amended claims (e.g., see claim 10). Likewise, the process taught by LaBerge is **performed under control of the CPU executing BIOS** during the initialization of a computer system (see Fig. 7; col. 3, lines 6-16; col. 4, lines 36-65, relied on by the Office Action for rejection). Unlike the AAPA relating to determination of a **common write delay time for writing data to a memory**, LaBerge discloses embodiments relating to data strobe signals for a **timing sequence of a memory read operation** (see col. 3, lines 7-28; col. 4, lines 20-35). Further, what LaBerge actually teaches in the cited passage is to find the beginning and end of the preamble of a DQS_OUT signal by programming a delay 79 by a processor 32. The **delay 79 to be programmed and adjusted during the process** taught in the cited passage ***is not*** the claimed "**write delay time**" (see FIGS. 8-12 to identify delay 79). In this regard, the passage relied on by the Office Action actually states:

> **The delay 79 may be programmed by the processor 32** (via lines 63 that are coupled to a configuration register) **when executing basic input/output system (BIOS) code** after initial bootup of the computer system 30. Referring also to FIG. 14, in this manner, the **processor 32** may initially program the strobe enable circuit 62 (via a register of the north bridge 34) with a value to set the delay 79 to approximately zero, and thereafter, the **processor 32 may initiate a series of write and read operations to determine if the beginning of the preamble has been located**.

(*Emphasis added,* col. 4, lines 36-45)

The teaching of LaBerge above, as well as AAPA, contrasts with the amended claims (e.g., claim 10) requiring that for determining a common write delay time of a memory, **a write command is directly issued from said north bridge chipset to said memory so as to write a pattern to said memory according to a write delay time**. The teaching of the two cited references also contrasts with amended claim 5 requiring "**directly writing said pattern into said corresponding block by said north bridge chipset according to said write command after said selected write delay time has elapsed,**" in step (b). For at least these reasons, the rejections should be withdrawn.

LaBerge also provides an example for **determining if the beginning of the preamble has been located** in the cited passage as follows:

> For example, the **processor 32 may (via the north bridge 34) write** (block 102) **a pattern of test data to predefined locations of the system memory 44**. The processor 32 then may read (block 104) the contents of the predefined locations and compare the read data with the original pattern to determine if a read error occurred. If so, **the processor 32 makes (block 108) coarse adjustments to increase the delay and repeats blocks 102 and 104 until no read errors occur. The processor 32 then makes fine adjustments to decrease the delay and repeats blocks 102 and 104 until a read error occurs, an event that identifies the beginning of the preamble**. At this point, the processor 32 determines (diamond 106) that the beginning of the preamble has been located and then performs read and write operations similar to those described above to find the end of the preamble. In this manner, after the processor 32 determines (diamond 110) that the end of the preamble has been located, the processor 32 programs (block 112) the strobe enable circuit 62 with the appropriate value. The duration of the delay 79 may vary over time due to, for example, temperature and voltage fluctuations.

(*Emphasis added*, col. 4, lines 45-65)

A noticeable difference in the example is that **after setting the delay 79 to a particular value**, the **processor 32** (not the north bridge 34) **controls the writing of a pattern of test data** to the system memory 44 and then reads the pattern from the system memory 44.

For at least the foregoing reasons, the AAPA and LaBerge collectively fail to disclose all features of the claims as amended. In addition, nothing in either of the cited references suggests the combination proposed by the Office Action. It is noted that the Office Action relies on Figure 7 of LaBerge and asserts that "it is more advantageous to utilize the north bridge in determining and adjusting the write delay time of a memory because the north bridge is physically more closer to the processor and the system memories [Fig. 7]" in order to support the assertion of nonobviousness. However, Figure 7 is only a structure of a computer system and nothing in Figure 7 suggests one of ordinary skill in the art to combine the AAPA and LaBerge and modify such combination to arrive at the claimed invention.

In particular, and as described above, the delay 79 of LaBerge is not the write delay time of AAPA, while both AAPA and LaBerge require the CPU executing the BIOS to perform different processes for their respective intended purposes. Such combination would not arrive at claim 10 requring "**directly issuing, from said north bridge chipset, a write command to said memory so as to write a pattern to said memory according to a write delay time.**" Regarding amended claim 5, such combination also would not arrive at claim 5, as required above.

According to MPEP 2143, "**[t]he *teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure*.**" As above discussed, no such suggestion or motivation is found in the prior art to one of ordinary skill in the art at the time of the invention to combine the cited references to arrive at the rejected claims, as in claims 5 and 10. For at least this reason, it is respectfully submitted that a prima facie case of obviousness has not been established, and the rejection of the independent claims (e.g., claims 5 and 10) be withdrawn.

Moreover, as a separate reason as to patentability of amended claims 5 and 10, even if the AAPA and LaBerge were combined, in view of the above discussed differences among the cited references and the rejected claims, as in claims 5 and 10, one would recognize that the combination could not arrive at the rejected claims unless the combination would require a substantial redesign of at least the sequence of operations of the CPU and BIOS, as well as their respective roles, in determining a common write delay time in the AAPA, during initialization of a computer system. However, in addition to a merely conclusory description that the AAPA and LaBerge would be combined, nothing in the Office Action mentions what the proposed combination would be, how it would work, and how it would result in the claimed invention. Accordingly, it is respectfully submitted that claims 5 and 10 distinguish over the cited references, whether taken individually or in combination.

Since independent claims 1 and 7 include the features similar to those of claim 10, as well as additional features, individually, it is respectfully submitted that claims 1 and 7 distinguish over the cited references, whether taken individually or in combination, for the same rationale to amended claim 10. Likewise, as the Office Action has set forth only a single brief discussion of the prior art to apply equally to each of claims 1, 5, 7, and 10, the foregoing discussion (concentrated on claims 5 and 10) is sufficient to properly respond to the rejection, with respect to all claims.

As all remaining claims depend from either independent claims 1, 5, 7, or 10, these dependent claims also define over the prior art for at least the same reasons.

Conclusion

For the foregoing reasons, it is respectfully submitted that this application with claims 1-13 is in condition for allowance. Notice of such allowance and passing of the application to issue, are earnestly requested. Should the Examiner feel that a conference would be helpful in expediting the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

A credit card authorization is provided to cover the fee associated with the accompanying request for extension of time. No additional fee is believed to be due in connection with this amendment and response to Office Action. If, however, any additional fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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